Remarks:

Reconsideration of the application is requested.

Claims 1 and 5-15 are now in the application. Claims 1 and 5 have been amended. Claims 2-4 have been cancelled and claims 11-15 have been added.

Regarding item 2 on page 2 of the Office action, it is noted that the instant application is a continuation of the PCT application.

In item 4 on pages 2-3 of the above-identified Office action, the drawings have been objected to as not showing every feature of the invention specified in the claims.

More specifically, the Examiner has stated that the limitation "at least one second capacitive element is one of a plurality of second capacitive elements" in claim 3 and the limitation "at least one second capacitive element is formed by an interaction of said at least one third supply track and said first supply track" in claim 7 must be shown or the features(s) cancelled from the claim(s).

A new Fig. 3 has been added, which shows a second capacitive element formed by an interaction of a first supply track 1 and

a third supply track 3. The corresponding parts of the specification have been changed accordingly.

In item 5 on pages 3-8 of the above-mentioned Office action, claims 1-10 have been rejected as being unpatentable over Dasgupta (US Pat. No. 6,146,939) under 35 U.S.C. § 103(a).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. More specifically, the features of claims 2-4 have been added to claim 1 and Claims 2-4 have been cancelled. Support for the changes may also be found on page 11, lines 4-7, page 14, lines 12-19, page 15, lines 11-13, and page 17, lines 1-15 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> **said first supply track and said second supply track forming a first metallic layer;**
> said second capacitive elements each having a capacitance and said first capacitive elements each having a capacitance having **at least a factor of 10 greater** than said capacitance of said second capacitive elements; and said at least one first capacitive element and said at least one second capacitive element being connected in parallel and **smoothing over** the supply voltage.

Dasgupta discloses a metal-polycrystalline silicon-n-well multiple layered capacitor. The invention of the instant application differentiates from Dasgupta in at least the following aspects:

1) There are large possibilities for the components that can be used as supply tracks. In the invention of the instant application, the first metal layer is used as supply tracks 1 and 2. This is not disclosed in Dasgupta and cannot be considered obvious from Dasgupta.

2) Although different capacitances can be assumed to have different capacitive components and resistive components, the ratio of at least 10 according to the invention of the instant application cannot be considered only as routine experimentation and optimization. The object of the invention of the instant application is to smooth over a supply voltage particularly in the case of high-frequency signals. As can be seen from Fig. 2B and the detailed description on page 18, line 10 to page 19, line 20 of the specification of the instant application, the ratio of the capacitances of the first and second capacitive elements leads to a special effectiveness, that is a smoothing which is effective in an especially large frequency range. Since the smoothing of the supply voltage is not an object of Dasgupta, there is no reason for a person skilled in the art to receive a hint from

Dasgupta to reach the invention of the instant application.

Clearly, Dasgupta does not show "**said first supply track and said second supply track forming a first metallic layer**; said second capacitive elements each having a capacitance and said first capacitive elements each having a capacitance having **at least a factor of 10 greater** than said capacitance of said second capacitive elements; and said at least one first capacitive element and said at least one second capacitive element being connected in parallel and **smoothing over** the supply voltage", as recited in claim 1 of the instant application.

Claim 1 is, therefore, believed to be patentable over Dasgupta and since claims 5-10 are ultimately dependent on claim 1, they are believed to be patentable as well.

For the same reasons as discussed above, the new claims 11-15 are believed to be patentable.

In view of the foregoing, reconsideration and allowance of claims 1 and 5-15 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicants

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Marked-Up Version of the Amended Paragraphs in the Specification and Marked-Up Version of the Amended Claims:

The paragraph starting on page 8, line 17 and ending on page 8, line 19 now reads as:

Fig. 1 is a diagrammatic, sectional view of a basic structure of an integrated circuit having capacitive elements provided for smoothing a supply voltage according to the invention, wherein a second capacitive element is formed by an interaction of the second supply track and the third supply track;

The paragraph starting on page 8, line 21 and ending on page 8, line 22 now reads as:

Fig. 2a is a circuit diagram [of] for the elements of the integrated circuit shown in Fig. 1 and Fig. 3; [and]

The paragraph starting on page 8, line 24 and ending on page 8, line 25 now reads as:

Fig. 2b is a graph showing associated impedance curves of the integrated circuit[.]; and

Claim 1(amended). An integrated circuit, comprising:

a first supply track to be connected to a first supply potential;

a second supply track to be connected to a second supply potential, the first supply potential and the second supply potential supplying a supply voltage, said first supply track and said second supply track forming a first metallic layer;

at least one second metallic layer having at least one third supply track to be connected to one of the first supply potential and the second supply potential and disposed in each case above said first metallic layer; [and]

at least one first capacitive element disposed below said first metallic layer; and

at least one second capacitive element defined by said at least one third supply track and at least one of said first supply track and said second supply track [defining at least one second capacitive element,];

said at least one first capacitive element and said at least one second capacitive element being connected in parallel and smoothing over the supply voltage;

said at least one first capacitive element being one of a plurality of first capacitive elements disposed below both said first supply track and said second supply track, and said at least one second capacitive element being one of a plurality of second capacitive elements;

said second capacitive elements each having a capacitance and said first capacitive elements each having a capacitance having at least a factor of 10 greater than said capacitance of said second capacitive elements.

Claim 5(amended). The integrated circuit according to claim [3] 1, including:

a substrate having doping regions formed therein; and

a polysilicon layer having at least one poly section disposed above said substrate, said first capacitive elements formed by an interaction of said at least one poly section formed in said polysilicon layer and said doping regions formed in said substrate.